CLAIM AMENDMENTS

Please amend the claims (~~strikethrough~~ indicating deletion and underline indicating insertion) as follows:

1. (Previously Presented) A multi-phase sampling system having an odd number of evenly distributed clock phases, the clock phases being generated by a multi-phase clock generator, the system comprising:

a plurality of samplers, each of the samplers sampling a same input data signal when a clock signal of one of the respective phases is received by the respective sampler, each sampler sampling a portion of the input data signal corresponding to a transition of the input data signal and a portion of the input data signal corresponding to data, the portion of the input data signal corresponding to data being in between two consecutive transitions of the input data signal, each sampler outputting a respective output signal.

2. (Original) The multi-phase system of claim 1, wherein the multi-phase system comprises an odd number of said samplers.

3. (Original) The multi-phase system of claim 1, further comprising:

phase error determination circuitry, the phase error determination circuitry receiving the respective output signals and making a respective phase error determination based on each of the respective output signals.

4. (Original) The multi-phase system of claim 3, further comprising:

phase shifting circuitry, the phase shifting circuitry shifting one or more of the phases in accordance with the respective phase error determinations.

5. (Original) The multi-phase system of claim 1, wherein the multi-phase system is a receiver in communication with a multi-phase transmitter.

6. (Original) The multi-phase system of claim 1, wherein the multi-phase system is a transmitter.

7. (Original) The multi-phase system of claim 5, wherein the multi-phase system further comprises:

phase error determination circuitry, the phase error determination circuitry receiving the respective output signals and making a respective phase error determination based on each of the respective output signals, and wherein some of the phase error determinations correspond to phase errors of the multi-phase receiver and wherein some of the phase error determinations correspond to phase errors of the multi-phase transmitter.

8. (Original) The multi-phase system of claim 7, further comprising:

phase shifting circuitry, the phase shifting circuitry shifting one or more of the phases of the multi-phase receiver in accordance with the respective phase error determinations.

9. (Original) The multi-phase system of claim 7, wherein the phase error determinations that correspond to phase errors of the multi-phase transmitter are fed back to the multi-phase transmitter to enable phase shifting circuitry of the multi-phase transmitter to shift one or more of the phases of the multi-phase transmitter in accordance with the respective phase error determinations of the multi-phase transmitter.

10. (Previously Presented) A multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, the apparatus comprising:

a first sampling device that receives a first data signal and the first clock signal,

the first sampling device comprising first sampling logic configured to sample the first data signal when the first clock signal is received by the first sampling device and to cause a first output signal to be output from the first sampling device, the first sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

a second sampling device that receives the first data signal and the second clock signal, the second sampling device comprising second sampling logic configured to sample the first data signal when the second clock signal is received by the second sampling device and to cause a second output signal to be output from the second sampling device, the second sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

a third sampling device that receives the first data signal and the third clock signal, the third sampling device comprising third sampling logic configured to sample the first data signal when the third clock signal is received by the third sampling device and to cause a third output signal to be output from the third sampling device, the third sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

phase error determination circuitry configured to determine a first phase error indication associated with the first output signal, a second phase error indication associated with the second output signal and a third phase error indication associated with the third output signal; and

phase shifting circuitry configured to shift at least one of the first, second or third phases in accordance with the respective first, second, or third phase error indications.

11. (Original) The apparatus of claim 10, wherein at least the first phase error indication is used by the phase shifting circuitry to phase-lock the multi-phase clock signal generator, and wherein the phase shifting logic shifts the second and third phases in accordance with the second and third phase error indications, respectively.

12. (Original) The apparatus of claim 10, wherein the first, second and third phase error indications are used by the phase shifting circuitry to phase-lock the multi-phase clock signal generator, and wherein the phase shifting circuitry shifts the first, second and third phases in accordance with the first, second and third phase error indications, respectively.

13. (Original) The apparatus of claim 10, wherein the phase shifting circuitry includes first, second and third charge pumps that perform modulo binning of the first, second and third phase error indications, respectively, to obtain first, second and third phase shifting values, and wherein the phase shifting circuitry shifts the first, second and third phases in accordance with the obtained first, second and third phase shift values, respectively.

14. (Original) The apparatus of claim 10, wherein the phase error determination circuitry comprises logic that is configured based on an Alexander Phase Determination Truth Table algorithm.

15. (Original) The apparatus of claim 13, wherein the phase shifting logic further includes at least first and second phase shifters configured to operate on the first and second clock signals, respectively, the first and second phase shifters receiving outputs from the first and second charge pumps, respectively, the first and second phase shifters shifting the first and second phases, respectively, in accordance with the outputs received from the first and second charge pumps, respectively.

16. (Original) The apparatus of claim 15, wherein the apparatus is incorporated into a receiver, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points in time to thereby cause the first and second sampling devices to sample the first data signal at correct points in time, the first data signal corresponding to a signal transmitted by a transmitter.

17. (Original) The apparatus of claim 15, wherein the apparatus is comprised by a receiver, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points in time to cause the first and second sampling logic to optimally sample the first data signal, the first data signal corresponding to a signal transmitted by a transmitter, the transmitter being a multi-phase system comprising a multi-phase clock generator that generates at least third, fourth, fifth, sixth and seventh clock signals having third, fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and seventh phases being different from each other, and wherein the phase error determination logic is also configured to determine one or more phase error indications associated with events occurring in the transmitter, and wherein the phase error indications determined to be associated with events occurring in the transmitter are transmitted by the receiver to the transmitter to enable the transmitter to adjust the third, fourth, fifth, sixth and seventh phases to eliminate phase errors in the third, fourth, fifth, sixth and seventh clock signals.

18. (Original) The apparatus of claim 15, wherein the apparatus is comprised by a transceiver, the transceiver comprising a local receiver and a local transmitter, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points to cause the first and second sampling logic to optimally sample the first data signal, and wherein the first data signal corresponds to a signal transmitted by a remote transmitter, the remote transmitter being a multi-phase system comprising a multi-phase clock generator that

generates at least third, fourth, fifth, sixth and seventh clock signals having third, fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and seventh phases being different from each other, and wherein the phase error determination logic is also configured to determine one or more phase error indications associated with events occurring in the remote transmitter, and wherein the phase error indications determined to be associated with events occurring in the remote transmitter are transmitted by the receiver to the remote transmitter to enable the remote transmitter to adjust the third, fourth, fifth, sixth and seventh phases to eliminate phase errors in the third, fourth, fifth, sixth and seventh clock signals, respectively.

19. (Original) An apparatus for sampling signals in a first multi-phase system, the first multi-phase system comprising a multi-phase clock signal generator that generates *m* clock phases, each clock phase being different, the apparatus comprising:

n sampling devices, *m* and *n* being integers that are relatively prime, wherein *n* corresponds to a number of clock phases of a second multi-phase system and is equal to or greater than 3, each of the sampling devices sampling a first data signal when one of the *m* clock signals is received by the sampling device and outputting an output signal;

phase error determination circuitry, the phase error determination circuitry being configured to determine a phase error indication associated with each output of the *n* sampling devices;

m + *n* modulo binning devices, and wherein *m* of the modulo binning devices perform binning of the phase error indications associated with the outputs of the *m* sampling devices to obtain phase error adjustment values for the *m* clock phases, and wherein *n* of the modulo binning devices perform modulo binning of the phase error indications associated with the outputs of the *n* sampling devices to obtain phase error adjustment values for the *n* clock phases; and

phase shifting circuitry of the first multi-phase system configured to shift the *m* clock phases in accordance with the phase error adjustment values obtained for the *m* clock phases.

20. (Original) The apparatus of claim 19, wherein the first multi-phase system is a receiver and wherein the second multi-phase system is a transmitter, and wherein *m* is an odd number that is equal to or greater than 3.

21. (Original) The apparatus of claim 19, wherein the first multi-phase system is a receiver that includes routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said second multi-phase system, the second multi-phase system corresponding to a remote transmitter, and wherein the first data signal sampled by said *n* sampling devices corresponds to a signal transmitted by the remote transmitter.

22. (Original) The apparatus of claim 19, wherein the first multi-phase system is a transceiver, the transceiver comprising a local receiver and a local transmitter, the second multi-phase system corresponding to said local transmitter, the transceiver including routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said second multi-phase system, and wherein the first data signal sampled by said *n* sampling devices corresponds to a signal transmitted by the local transmitter.

23. (Original) An apparatus for controlling sampling operations in a first multi-phase system and in a second multi-phase system, the first multi-phase system comprising a first multi-phase clock signal generator that generates *m* clock signals of *m* different phases, the second multi-phase system comprising a second multi-phase clock signal generator that generates *n* clock signals of *n* different phases, *m* and *n* being integers that are relatively prime, the apparatus comprising:

n sampling devices of the first multi-phase system, each of the sampling devices sampling a data signal of the second multi-phase system when one of the *m* clock phase is received by the sampling device and outputting an output signal, and wherein *n* is equal to or greater than 3;

phase error determination circuitry of the first multi-phase system, the phase

error determination circuitry being configured to determine a phase error indication associated with each output of the sampling devices;

m + *n* modulo binning devices, wherein *m* of the modulo binning devices perform binning of the phase error indications associated with the outputs of the *m* sampling devices to obtain phase error adjustment values for the *m* clock phases, and wherein *n* of the modulo binning devices perform modulo binning of the phase error indications associated with the outputs of the *n* sampling devices to obtain phase error adjustment values for the *n* clock phases; and

phase shifting circuitry of the first multi-phase system configured to shift the *m* clock phases in accordance with the phase error adjustment values obtained for the *m* clock phases; and

phase shifting circuitry of the second multi-phase system configured to shift the *n* clock phases in accordance with the phase error adjustment values obtained for the *n* clock phases.

24. (Original) The apparatus of claim 23, wherein the first multi-phase system is a local receiver and the second multi-phase system is a remote transmitter, the apparatus being included in the first multi-phase system, and wherein the apparatus further comprises routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said second multi-phase system.

25. (Original) The apparatus of claim 23, wherein the first multi-phase system is a transceiver comprising a local receiver and a local transmitter, the second multi-phase system corresponding to the local transmitter, the transceiver including routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said local transmitter to be used by the phase shifting logic of the local transmitter to shift the *n* clock phases in accordance with the phase error adjustment values obtained for the *n* clock phases.

26. (Original) The apparatus of claim 23, wherein the phase error determination logic comprises logic that determines phase errors based on an Alexander Phase Determination Truth Table algorithm.

27. (Original) The apparatus of claim 23, wherein the modulo binning of the phase error indications is performed by delivering the phase error indications to respective charge pumps of the modulo binning devices in a round robin fashion.

28. (Previously Presented) A method for controlling clock phases in a multi-phase system, the multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, the method comprising the steps of:

sampling a first data signal with a first sampling device when the first clock signal is received by the first sampling device and outputting a first output signal from the first sampling device, the first sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

sampling the first data signal with a second sampling device when the first clock signal is received by the second sampling device and outputting a second output signal from the second sampling device, the second sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

sampling the first data signal with a third sampling device when the first clock signal is received by the third sampling device and outputting a third output signal from the third sampling device, the third sampling device sampling the first data signal at a

portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

determining at least a first phase error indication associated with the first output signal, a second phase error indication associated with the second output signal and a third phase error indication associated with the third output signal;

shifting at least one of the first, second or third phases in accordance with the respective first, second or third phase error indications.

29. (Original) The method of claim 28, further comprising the step of:

phase-locking the multi-phase clock signal generator in accordance with the first phase error indication, and wherein the shifting step includes shifting at least the second and third phases in accordance with the second and third phase error indications, respectively.

30. (Original) The method of claim 28, further comprising the step of:

phase-locking the multi-phase clock signal generator in accordance with the first, second and third phase error indications, and the shifting step includes shifting the first, second and third phases in accordance with the first, second and third phase error indications, respectively.

31. (Original) The method of claim 30, wherein the step of shifting the first and second phases includes utilizing at least first and second charge pumps to perform modulo binning of the first and second phase error indications, respectively, to obtain first and second phase shifting values and shifting the first and second phases in accordance with the obtained first and second phase shift values, respectively.

32. (Original) The method of claim 28, wherein the phase errors are determined based on an Alexander Phase Determination Truth Table algorithm.

33. (Original) A method for sampling signals in a first multi-phase system, the first multi-phase system comprising a multi-phase clock signal generator that generates *m* clock phases, each clock phase being different, the method comprising the steps of:

sampling a first data signal with *n* sampling devices, wherein *n* corresponds to a number of clock phases of a second multi-phase system and wherein *m* and *n* are integers that are relatively prime and *n* is equal to or greater than 3, each sampling device sampling the first data signal when one of the *m* clock signals is received by the respective sampling device and outputting an output signal;

determining a phase error indication associated with each output of the *n* sampling devices;

utilizing *m* + *n* modulo binning devices to perform binning of the phase error indications associated with the outputs of the *m* + *n* sampling devices to obtain phase error adjustment values for the *m* clock phases and phase error adjustment values for the *n* clock phases; and

shifting the *m* clock phases in accordance with the phase error adjustment values obtained for the *m* clock phases.

34. (Original) The method of claim 33, wherein the first multi-phase system is a receiver that includes routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said second multi-phase system, the second multi-phase system corresponding to a remote transmitter, and wherein the first data signal sampled by said *n* sampling devices corresponds to a signal transmitted by the remote transmitter.

35. (Original) The method of claim 33, wherein the first multi-phase system is a transceiver, the transceiver comprising a local receiver and a local transmitter, the transceiver including routing logic configured to cause the phase error adjustment values obtained for the *n* clock phases to be sent to said second multi-phase system, the second multi-phase system corresponding to said local transmitter, and wherein the

first data signal sampled by said *n* sampling devices corresponds to a signal transmitted by the local transmitter.

36. (Original) A method for controlling sampling operations in a first multi-phase system and in a second multi-phase system, the first multi-phase system comprising a first multi-phase clock signal generator that generates *m* clock phases, each clock phase being different, the second multi-phase system comprising a second multi-phase clock signal generator that generates *n* clock phases, each of the *n* clock phases being different, *m* and *n* being integers that are relatively prime, the method comprising the steps of:

sampling a data signal *n* sampling devices, each of the *n* sampling devices sampling the data signal upon receiving one of the *m* clock signals and outputting an associated output signal, and wherein *n* is equal to or greater than 3;

for each output signal, determining a corresponding phase error indication;

binning the phase error indications modulo *m* to obtain phase error adjustment values for the *m* clock phases;

binning the phase error indications modulo *n* and to obtain phase error adjustment values for the *n* clock phases; and

shifting the *m* clock phases in accordance with the phase error adjustment values obtained for the *m* clock phases; and

shifting the *n* clock phases in accordance with the phase error adjustment values obtained for the *n* clock phases.

37. (Previously Presented) A method for sampling data in multi-phase sampling system having an odd number of clock phases, the clock phases being generated by a multi-phase clock generator, the method comprising the steps of:

using an odd number of samplers to sample a common input signal, each sampler sampling the input signal when a clock signal of one of said phases is received thereby, each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal, each of the sampling devices outputting a respective output signal.

38. (Original) The method of claim 37, further comprising the steps of:

receiving the respective output signals and making a respective phase error determination based on each of the respective output signals.

39. (Original) The method of claim 38, further comprising:

shifting one or more of the phases in accordance with the respective phase error determinations.

40. (Previously Presented) A computer program for reducing clock phase errors in a multi-phase system, the computer program being embodied on a computer-readable medium, the multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, wherein first, second and third sampling devices of the multi-phase system sample a first data signal upon receiving the first, second and third clock signals, respectively, and outputting first, second and third output signals, respectively, each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of

the first data signal, the computer program comprising:

a first code segment for processing the first, second and third output signals and determining first, second and third phase error indications associated with the first, second and third output signals, respectively; and

a second code segment for determining an amount by which at least one of the first, second and third phases are to be shifted based on the first, second or third phase error indications, respectively.

41. (Original) The computer program of claim 40, wherein the first code segment corresponds to an Alexander Phase Determination Truth Table algorithm.